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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,631	01/24/2000	Yutaka Usami	00037/LH	7420

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EXAMINER
MAKHDOOM, SAMARINA

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/490,631	Applicant(s) USAMI ET AL.	
	Examiner Samarina Makhdoom	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7, 9-13, 15, 17-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Rohrer et al., U.S. Patent No. 5,313,398, May 17, 1994.

As per Claims 1-2, 9-10, and 17-18, Rohrer et al. teach a network simulating (See Col. 1, lines 49-63 for the circuit simulation having elements, connecting nodes, and electrical parameters like a network) method comprising the steps of:

defining element cells representing electric functions of a plurality of circuit elements and connection pipes representing wiring lines for connecting the circuit elements (See Col. 5, lines 48-67 for the microelectronic circuit design system that include libraries or macros for elements thereby defining the elements. Also see the wiring program that determines the interconnect paths between the elements. See Col. 12, lines 18-33 for the representation of the micro-electronic circuit that contains the netlist descriptions and the connection to each node in the circuit),

defining an electric network current as the number of particles moving in the connection pipe per unit time (See Col. 9 lines14-43 for the defining of the circuit current, current is the number of electrons or particles moving in a wire or connection pipe for a given time period),

and defining an electric network voltage as the number of particles present in the connection pipe (See Col. 9, lines 14-43 for the defining of the circuit voltage, voltage is the amount of electrons or particles present in the connection pipe or wire);

on the basis of definitions in the defining step, setting beforehand, in units of element cells, a rule for expressing an electric function of each of the circuit elements in accordance with a state of the connection pipe connected to each of the element cells (See Col. 5, lines 48-67 for a library defining each cell and its function; and a checking system that makes sure all the elements meet design constraints and design rules);

transferring particles between the element cell and the connection pipe in accordance with the set rule (See Col. 11, lines 1-11 for The model represents an analytical transfer function for the circuit which is useful when responses to repetitive forcing functions are being analyzed. This allows the interconnect characterization (or connection pipe characteristics) to be pre-processed for higher levels of simulation);

and simulating the state of the electric network by updating the number of particles passing through a given connection pipe per unit time in the transferring step and the number of particles present in the given connection pipe (See abstract for the calculation of the current vector (or number of particles or electrons passing through a connection pipe or wire) that is a function of time. The movement of particles represents the transferring step),

and performing transfer and updating processes at least once (See Col. 11, lines 1-11 for The model represents an analytical transfer function for the circuit which is useful when responses to repetitive forcing functions are being analyzed therefore the transfer process occurs at least one time).

As per Claims 3, 11, and 19, Rohrer et al. teach a setting step includes the step of when a given one of the circuit elements is a current source (See Col. 5, lines 48-67 for the circuit containing current sources),

setting a rule for extracting the number of particles corresponding to a current value Per unit time from one of two connection pipes connected to an element cell expressing the given circuit element and giving the number of particles equal in number to the number of extracted particles to the other one of the two connection pipes (See Col 15, lines 1-67 for the calculation of current or number of particles corresponding to a current value per unit time and see Equation 11. Also see Figure 10 for the time domain solution).

As per Claims 4, 12, and 20, Rohrer et al. teach a setting step includes the step of when a given one of the circuit elements is a voltage source (See Col. 5, lines 48-67 for the circuit containing voltage sources),

setting a rule for making a difference between the number of particles in one of two connection pipes connected to an element cell expressing the given circuit element and the number of particles in the other one of the two connection pipes equal to the number of particles corresponding to a voltage of the voltage source (See Col 15, lines 1-67 for the calculation of voltage or number of particles in the pipe corresponding to a voltage value per unit time and see Equation 11. Also see Figure 10 for the time domain solution).

As per Claims 5, 13, and 21, Rohrer et al. teach a defining step includes the step of when a given one of the element cells has non-linearity as a function of time (See Col. 10, lines 47-66 for defining nonlinear transient elements),

defining the given circuit element as a combination of an element cell for a resistive element and one of an element cell expressing a current source and an element cell expressing a voltage source, the combination expresses linearity equivalent to a behavior of the given circuit element at given time (See Col. 10, lines 14-66 for a matric for resistive elements, current and voltage sources, also see the linear equivalent based on the simulation time interval or per unit time);

and the setting step includes the steps of when a certain one of the circuit elements is a current source (See Col. 5, lines 48-67 for the circuit containing current sources),

setting a rule for extracting the number of particles corresponding to a current value per unit time from one of two connection pipes connected to an element cell expressing the certain circuit element and giving the number of particles equal in number to the number of extracted particles to the other one of the two connection pipes (See Col 15, lines 1-67 for the calculation of current or number of particles corresponding to a current value per unit time and see Equation 11. Also see Figure 10 for the time domain solution),

and when a specific: one of the circuit elements is a voltage source (See Col. 5, lines 48-67 for the circuit containing voltage sources),

setting a rule for making a difference between the number of particles in one of two connection pipes connected to an element cell expressing the specific circuit element and the number of particles in the other one of the two connection pipes equal to the number of particles corresponding to a voltage of the voltage source (See Col 15, lines 1-67 for the calculation of voltage or number of particles in the pipe corresponding to a voltage value per unit time and see Equation 11. Also see Figure 10 for the time domain solution).

As per Claims 7, 15, and 23, Rohrer et al. teach a transferring step and the simulating step include the step of simulating the state of each element cell at initial time so as to simulate a transient phenomenon of the given circuit element having non-linearity as a function of time (See Abstract for transient representation for the nonlinear elements for each simulation time),

simulating a behavior of the nonlinear element at an operating point advancing by a shortest time interval, by changing each parameter of a combination of the element cells having functions equivalent to the element cells (See Col. 3, lines 9-27, for simulation the behavior of nonlinear elements. Also See Col. 11, lines 1-11 for the simulation of nonlinear elements in the time domain or for the shortest time interval),

and simulating the transient phenomenon by repeating the change in parameter every time the shortest time interval has elapsed (See Figure 14, and Text in Col. 18, lines 41 et Seq. for the simulation of the transient response or phenomenon but repeating (see the looping in the flow chart) the change per increment of time 128).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 6, 8, 14, 16, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rohrer et al., in view of Going et al., U.S. Patent No. 6,271,579, August 7, 2001.

As per Claims 6, 8, 14, 16, 22, and 24, Rohrer et al. teach the limitations of Claims 1-2, 9-10, and 17-18 above as well as a setting step includes the step of:

preparing a plurality of rules for the element cell for expressing the given circuit element and selecting one of the plurality of rules in accordance with the state of the connection pipe connected to the element cell (See Col. 5, lines 47-67 for setting design rules and constraints for each circuit element).

simulating a behavior of the nonlinear element at an operating point advancing a shortest time interval by executing the transferring step in accordance with the rule selected in accordance with the state of the connection pipe connected to the element cell (See Col. 3, lines 9-27, for simulation the behavior of nonlinear elements. Also See Col. 11, lines 1-11 for the simulation of nonlinear elements in the time domain or for the shortest time interval),

and simulating the transient phenomenon by repeating the simulating steps every time the shortest time interval has elapsed (See Figure 14, and Text in Col. 18, lines 41 et Seq. for the

simulation of the transient response or phenomenon but repeating (see the looping in the flow chart) the change per increment of time 128).

Rohrer et al. Teach simulating resistance, admittance, and conductance but not impedance discontinuities.

Going et al., teach a circuit simulation for simulating discontinuous impedance (See Abstract for a trace determined by computer simulation to compensate for impedance discontinuities).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit simulator of Rohrer et al., with the impedance calculations of Going et al., because it would allow the Rohrer et al. simulator to be more accurate and simulate breaks in the connection wires.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Flint et al., U.S. Patent No. 6,141,634 disclose an AC Power Line Network simulator with an enclosure for containing elements of the system.

Lee, U.S. Patent No., 6,154,716 disclose improvement made to an electronic circuit simulator. The circuit is represented by a set of nodes and components.

Opal, A, "Sampled data simulation of linear and nonlinear circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.: 15 Issue: 3 , Mar 1996 Pages: 295 –307

Chang et al. "Transient analysis of VLSI interconnects with arbitrary initial distributions and nonlinear terminations," IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedings 10-12 Oct 1994, Pages: 563 –566.

Schutt-Aine, J.E., "Latency insertion method (LIM) for the fast transient simulation of large networks," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol.: 48 Issue: 1 , Jan 2001, Page(s): 81 –89.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Full Time on Tuesday, Thursday, Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
December 22, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER